IN THE CLAIMS

Please amend the following claims:

1-4. (Cancelled).

5. (currently amended) A software driven emulation engine, ~~for verifying functionality of logic designs~~ comprising:

~~at least one a module, said module comprising~~ a plurality of clusters, each including:

a data memory having a set of read ports; and

a plurality of processors ~~that execute~~ for executing logic gate functions from a logic design, ~~said processors organized into a plurality of clusters such that each of said plurality of clusters comprise a subset of said plurality of processors,~~ each of said processors ~~in each of said clusters~~ having a set of read addresses and accessing said ~~a~~ data memory ~~within each of said clusters~~; and

a time division multiplexer associated with each of said clusters coupling ~~a~~ said set of read ports of said data memory to a said set of read addresses of one processor of said cluster during one read cycle of said data memory and coupling said set of read ports of said data memory to a set of read addresses of another processor of said cluster during the next read cycle of said data memory,

wherein said plurality of clusters and said time division multiplexer thereby verify a functionality of the logic design.

6. (currently amended) The ~~A~~ software driven emulation engine of ~~as in~~ claim 5, wherein said data memory has an operating clock rate for read operations that is twice ~~the~~ an operating clock rate of said ~~module~~ processors.

7. (currently amended) A software driven emulation engine, ~~for verifying functionality of logic designs~~ comprising:

~~at least one module, said module including~~ a plurality of clusters, ~~wherein~~ each ~~of said clusters comprise~~ including:

a data memory having first and second sets of read ports; and

a plurality of processors ~~that execute~~ for executing logic gate functions from a logic design, each of said processors of each of said clusters having a set of read addresses and accessing said ~~a~~ data memory within each of said clusters;

a first time division multiplexer associated with each of said clusters that couples said ~~a~~ first set of read ports of said data memory to said ~~a~~ set of read addresses of a first processor of said cluster during one read cycle of said data memory and coupling said first set of read ports of said data memory to said ~~a~~ set of read addresses of a second processor in said cluster during the next read cycle of said data memory; and

a second time division multiplexer associated with each of said clusters that couples said ~~a~~ second set of read ports of said data memory to said ~~a~~ set of read addresses of a third processor of said cluster during said one read cycle of said data memory and coupling said second set of read ports ~~of a~~ to said set of read addresses of a fourth processor in said cluster during said next read cycle of said data memory,

wherein said plurality of clusters, said first time division multiplexer, and said second time division multiplexer verify a functionality of the logic design.

8. (currently amended) The ~~A~~ software driven emulation engine of ~~as in~~ claim 7, wherein said data memory has an operating clock rate for read operations that is twice ~~the~~ an operating clock rate of said ~~module~~ processors.

9. (currently amended) A emulation engine, ~~for verifying functionality of logic designs~~ comprising:

~~at least one module, said module comprising~~ a plurality of clusters, said clusters each comprising:

a data memory having a set of read ports; and

a plurality of processors ~~that that execute~~ for executing logic gate functions from a logic design, each of said processors within each of said clusters accessing said ~~a~~ data memory within each of said clusters; and

a time division multiplexer associated with each of said clusters ~~that couples a~~ coupling said set of read ports of said data memory to a set of read addresses of one processor within a first of said clusters during one read cycle of said data memory and coupling said set of read ports of said data memory to a set of read addresses of another processor within said first of said clusters during the next read cycle of said data memory,

wherein said plurality of clusters and said time division multiplexer verify a functionality of the logic design.